Claims

[1] An FIR filter comprising a plurality of input delay circuits which are mutually connected in cascade and each of which delays the input data and outputs it, and a plurality of multiplier circuits each of which multiplies respective input data of said plurality of input delay circuit and the output data of the input delay circuit of the final stage by respective coefficients to make partial output data, and which sums up partial output data of said plurality of multiplier circuits to make filter output data, characterized in that

said FIR filter comprises a plurality of element circuits which have one or more input delay circuits each of which is configured by dividing said plurality of input delay circuits mutually connected in cascade in the direction of the cascade, and one or more multiplier circuits connected to said one or more input delay circuits, and which obtain partial sum data from partial output data of said one or more multiplier circuits,

and among said plurality of element circuits, the initial stage element circuit outputs said partial sum data directly, and each of the succeeding element circuits from the second stage outputs the partial sum data obtained by adding delayed said partial sum data obtained inside that element circuit to partial sum data output by the element circuit of the prior stage, and the element circuit of the final stage outputs the partial sum data as the filter output data.

[2] A FIR filter according to claim 1, characterized in that it comprises one initial stage element circuit which has one or more of said input delay circuits mutually connected in cascade into which filter input data is input, and said one or more of said multiplier circuits each of which multiplies each of the input data of said one or more input delay circuits by respective coefficient to make partial output data, and a partial output adder which adds partial output data of said one or more multiplier circuits mutually to make partial sum data,

one or more intermediate stage element circuits each of which has one

or more of said input delay circuits mutually connected in cascade into which the output data of said initial stage element circuit or the output data from the final input delay circuit of said intermediate stage element circuit of the prior stage is input, and said one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more of said input delay circuits by respective coefficient to make partial output data, and a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data, and a partial sum delay circuit which delays the partial sum data of said partial output adder, and a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data and

a final stage element circuit which has one or more of said plurality of input delay circuits mutually connected in cascade into which the output data from the final input delay circuit of said intermediate stage element circuit of the prior stage is input, and said plurality of multiplier circuits each of which multiplies each one of the input data from one or more of said plurality of input delay circuits and the output data from the final stage of the input delay circuit by respective coefficient to make partial output data, and a partial output adder which adds the partial output data from said plurality of multiplier circuits mutually to make partial sum data, a partial sum delay circuit which delays the partial sum data of said partial output adder, and a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said intermediate stage element circuit to make the filter output data.

[3] A FIR filter according to claim 2 characterized in that it comprises a plurality of element circuit sets each of which corresponds to the respective one of a plurality of divided input data divided from the original filter input data, each element circuit set is composed of said initial stage element circuit, said intermediate stage element

circuit, and said final stage element circuit, and among the plurality of element circuit sets, said coefficients of said multiplier circuits of all the element circuits corresponding to the same stage are made equal, and it comprises a filter output adder which aligns the decimal points and sums up the partial output data as a filter output data output by said final stage element circuit of said plurality of element circuit sets, and outputs the filter output data having a bit length corresponding to that of the original input data.

[4] A FIR filter according to claim 2 or 3 characterized in that said coefficients of said multiplier circuits are variable.

[5] An element circuit for an FIR filter according to any one of the claims 1 to 4 characterized in that it has one or more of said input delay circuits mutually connected in cascade,
one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more input delay circuits by respective coefficient to make partial output data and
a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data.

[6] An element circuit for an FIR filter according to any one of the claims 1 to 4 characterized in that it has one or more of said input delay circuits mutually connected in cascade,
one or more of said multiplier circuits each of which multiplies each one of the input data from said one or more input delay circuits by respective coefficient to make partial output data,
a partial output adder which adds the partial output data from said one or more multiplier circuits mutually to make partial sum data,
a partial sum delay circuit which delays the partial sum data of said partial output adder and
a partial sum adder which adds partial sum data delayed by said partial sum delay circuit and partial sum data of said initial stage element circuit or said intermediate stage element circuit of the prior stage to make partial sum data.

[7] An element circuit for an FIR filter according to any one of the

claims 1 to 4 characterized in that it has one or more of said input delay circuits mutually connected in cascade,

one or more of said multiplier circuits each of which multiplies the input data from said one or more input delay circuits the output data from the input delay circuit of the final stage by respective coefficient to make partial output data,

a partial output adder which adds the partial output data from one or more of said multiplier circuits mutually to make partial sum data,

a partial sum delay circuit which delays the partial output data of said partial output adder and

a partial sum adder which adds the partial sum data delayed by said partial sum delay circuit and the partial sum data of said intermediate stage element circuit of the prior stage to make filter output data.

[8] An element circuit for an FIR filter according to claim 6 characterized in that said element circuit for an FIR filter is substituted by at least one of said initial stage element circuit and said final stage element circuit.

[9] An element circuit for the FIR filter according to any one of the claims 5 to 8 characterized in that said coefficients of said multiplier circuits are variable.